DATA SHEET

SAA7740H
Digital Audio Processing IC (DAPIC)

Product specification
Supersedes data of 1996 Mar 11
File under Integrated Circuits, IC01

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Philips Semiconductors

PHILIPS

Digital Audio Processing IC (DAPIC) SAA7740H

FEATURES

Hardware

- Two digital inputs and two digital outputs in the I²S-bus format (i.e. 4 audio channels)
- Independent input/output interfaces
- Slave input/output interfaces
- Slave processing
- I²C-bus microcontroller interface
- DC filtering at the inputs
- One programmable 2nd-order digital filter unit
- Two multiply accumulate processor units (24 × 16-bit/MAC)
- DRAM interface and address computation unit for external delay lines
- On-chip coefficient and external delay line address storage
- Hardware controlled soft mute via the MUTE pin
- Hardware controlled soft demute via the $\overline{\text{RST}}$ pin
- Operating ambient temperature; –40 to +85 °C.

Software

- 5-band parametric equalizer with selectable centre frequency, slope setting and boost/cut gain settings from –12 to +12 dB
- Stereo width control from mono to stereo to spatial stereo
- Stereo Hall-effects for field acoustics, such as concert halls, with 8 coefficients and 8 delayed taps per channel
- External delay line processing for delays up to 1 second
- Reverberation with selectable reverberation time (up to 5 seconds) and energy
- Three different surround sound programs to obtain a spatial effect on 4 loudspeakers
- Passive DOLBY surround processing with the addition of an external dynamic noise reduction IC
- Karaoke processing
- Dual 16th-order correction filtering
- Quad 8th-order correction filtering
- Digital volume and balance control
- Soft controlled soft mute/demute via the microcontroller interface
- Input switching matrix
- Output rear and front switching matrix.

APPLICATIONS

- Digital amplifiers
- Audio combination sets
- Car audio systems
- TV audio channels.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DD(tot)}$	total DC supply voltage	all V_{DD} pins	4.5	5.0	5.5	V
$I_{DD(tot)}$	total DC supply current	f_{xtal} = 16.9344 MHz	–	60	–	mA
f_{xtal}	input crystal frequency		12.288	16.9344	23.0	MHz
P_{tot}	total power dissipation	f_{xtal} = 16.9344 MHz	–	0.3	–	W
T_{amb}	operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7740H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

BLOCK DIAGRAM

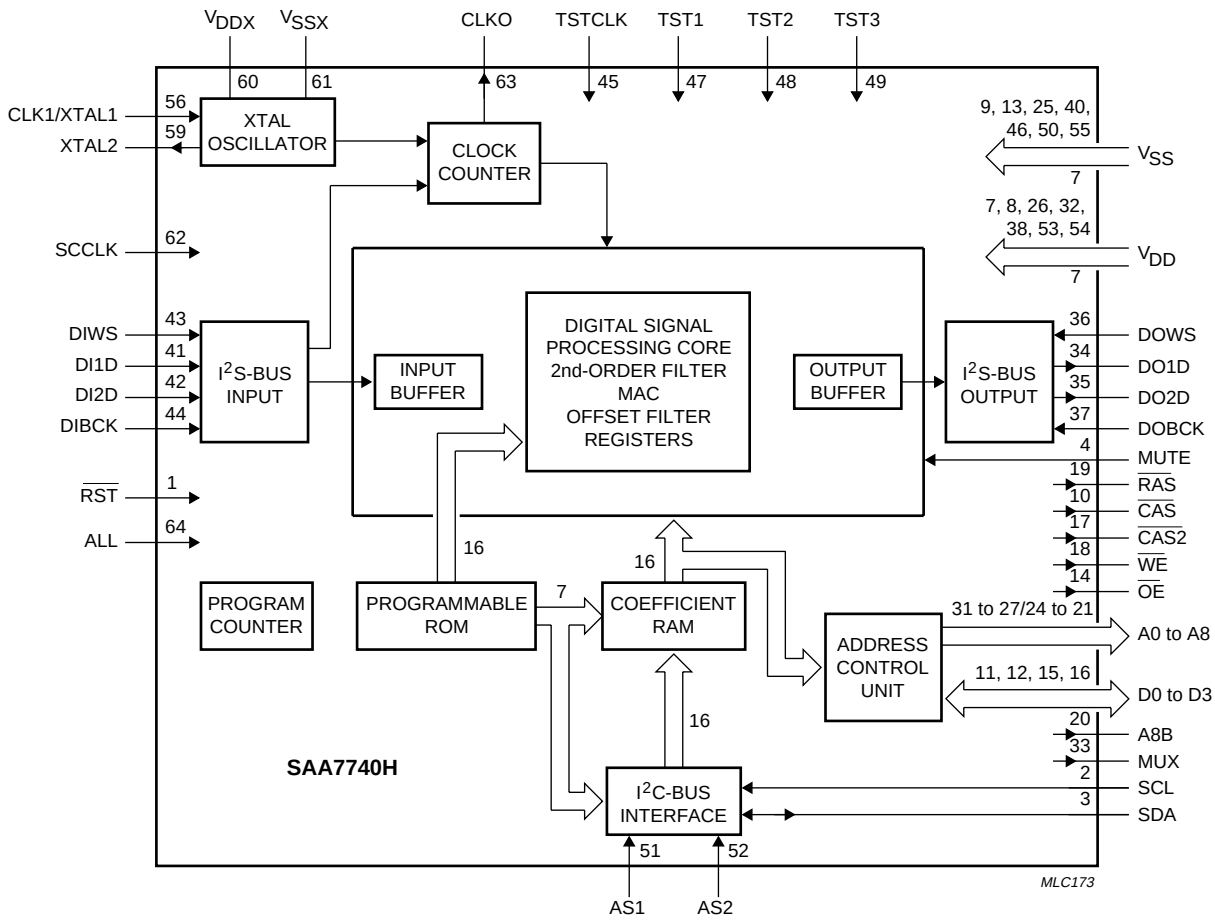


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{RST}$	1	reset input (active LOW)
SCL	2	serial clock input (I^2C-bus)
SDA	3	serial data input/output (I^2C-bus)
MUTE	4	mute input (active HIGH)
n.c.	5	not connected
n.c.	6	not connected
V_{DD}	7	supply voltage
V_{DD}	8	supply voltage
V_{SS}	9	ground supply
$\overline{CAS}$	10	column address strobe (DRAM) (active LOW)
D0	11	input/output data bus line 0 (DRAM)
D1	12	input/output data bus line 1 (DRAM)
V_{SS}	13	ground supply
$\overline{OE}$	14	output buffer enable (DRAM) (active LOW)
D2	15	input/output data bus line 2 (DRAM)
D3	16	input/output data bus line 3 (DRAM)
$\overline{CAS2}$	17	second column address strobe (active LOW)
$\overline{WE}$	18	write enable (DRAM; active LOW)
$\overline{RAS}$	19	row address strobe (DRAM; active LOW)
A8B	20	inverse MSB address line output (DRAM)
A8	21	address line output 8 (DRAM)
A7	22	address line output 7 (DRAM)
A6	23	address line output 6 (DRAM)
A5	24	address line output 5 (DRAM)
V_{SS}	25	ground supply
V_{DD}	26	supply voltage
A4	27	address line output 4 (DRAM)
A3	28	address line output 3 (DRAM)
A2	29	address line output 2 (DRAM)
A1	30	address line output 1 (DRAM)
A0	31	address line output 0 (DRAM)
V_{DD}	32	supply voltage
MUX	33	address latch strobe output (SRAM)

SYMBOL	PIN	DESCRIPTION
DO1D	34	digital audio output 1 (I^2S-bus)
DO2D	35	digital audio output 2 (I^2S-bus)
DOWS	36	digital audio input word select
DOBCK	37	digital audio input serial bit clock
V_{DD}	38	supply voltage
n.c.	39	not connected
V_{SS}	40	ground supply
DI1D	41	digital audio input 1 (I^2S-bus)
DI2D	42	digital audio input 2 (I^2S-bus)
DIWS	43	digital audio input word select
DIBCK	44	digital audio input serial bit clock
TSTCLK	45	clock input for test mode (should be tied LOW)
V_{SS}	46	ground supply
TST1	47	test pin input 1 (should be tied LOW)
TST2	48	test pin input 2 (should be tied LOW)
TST3	49	test pin input 3 (should be tied LOW)
V_{SS}	50	ground supply
AS1	51	address select input 1 (I^2C-bus)
AS2	52	address select input 2 (I^2C-bus)
V_{DD}	53	supply voltage
V_{DD}	54	supply voltage
V_{SS}	55	ground supply
CLK1/ XTAL1	56	clock or crystal input
n.c.	57	not connected
n.c.	58	not connected
XTAL2	59	crystal output 2
V_{DDX}	60	crystal supply voltage
V_{SSX}	61	crystal ground supply
SCCLK	62	scan test clock input (should be tied LOW)
CLKO	63	clock signal output
ALL	64	mode select input (should be tied HIGH)

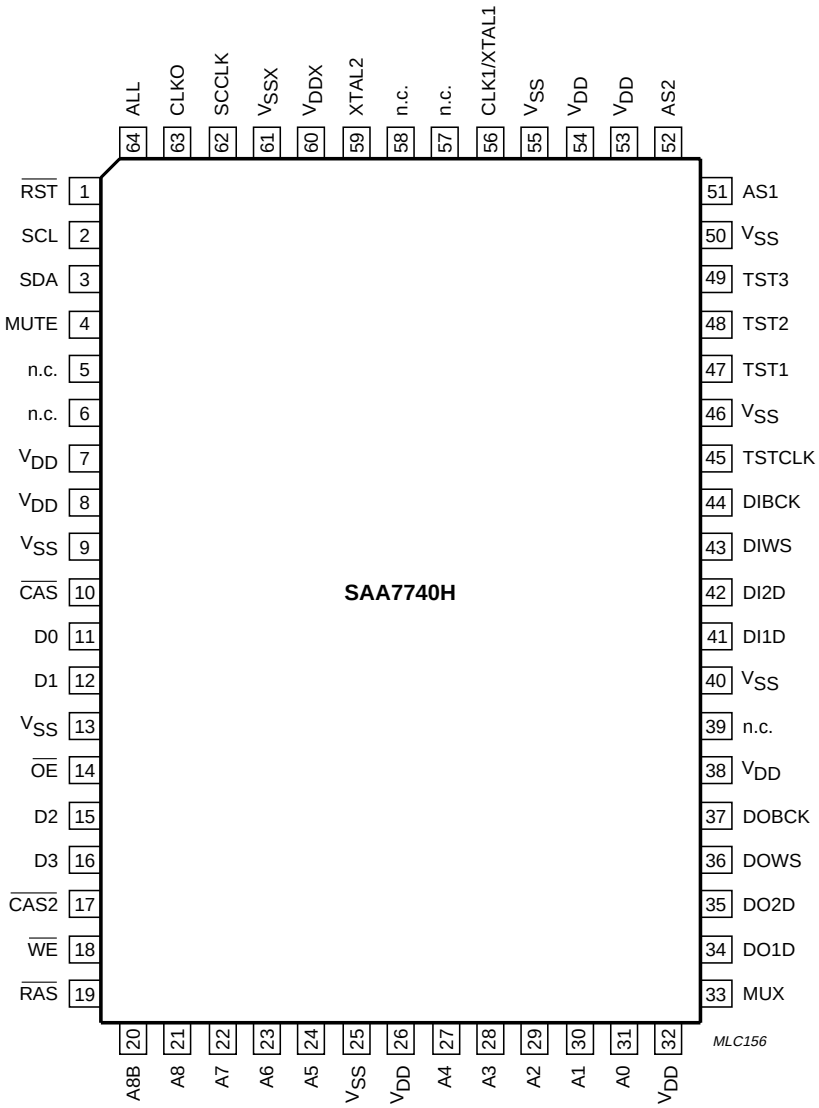


Fig.2 Pin configuration.

GENERAL DESCRIPTION

The SAA7740H is a function-specific digital signal processor. The device is capable of performing processing for listening-environments such as equalization, hall-effects, reverberation, surround-sound and digital volume/balance control. The SAA7740H can also be reconfigured (in a dual and quad filter mode) so that it can be used as a digital filter with programmable characteristics.

For reasons of silicon efficiency, the SAA7740H realises most functions directly in hardware. The flexibility exists in the possibility to download function parameters, correction coefficients and various configurations from a host microcontroller (see Fig.1). The parameters can be passed in real time and all functions can be switched on simultaneously.

The communication with a host microcontroller conforms with the standard I^2C-bus format. The SAA7740H accepts 2 digital stereo signals in the I^2S-bus format at audio sampling frequency (f_{as}) and provides 2 digital stereo outputs.

Mode description

The SAA7740H can be set in four basic modes of operation.

GENERAL DAPIC MODE

In the general DAPIC mode two variants are available (see Figs 3 and 4). In this mode the DAPIC accepts 2 stereo input signals. DC filtering is performed on the inputs before further processing. On one of the stereo inputs a 5-band graphic equalization can be performed. The stereo image of this signal can be controlled from mono to stereo.

In the first variant (see Fig.3) a stereo hall-effect can be added to the signal by means of direct reflections. In the second variant (see Fig.4) a reverberation effect can be added to the signal by means of exponential decaying reflections. Surround-sound can then be created for the rear loudspeakers. The surround-sound module is also able to provide karaoke.

The surround-sound module accepts the second stereo input, a microphone signal can be added via the 5-band equalizer. At the output, each of the 4 channels can be individually delayed via the external DRAM.
The interfacing and addressing of the DRAM is performed by the DAPIC.

The applications for the general mode are digital amplifiers, audio combination sets and TV audio channels.

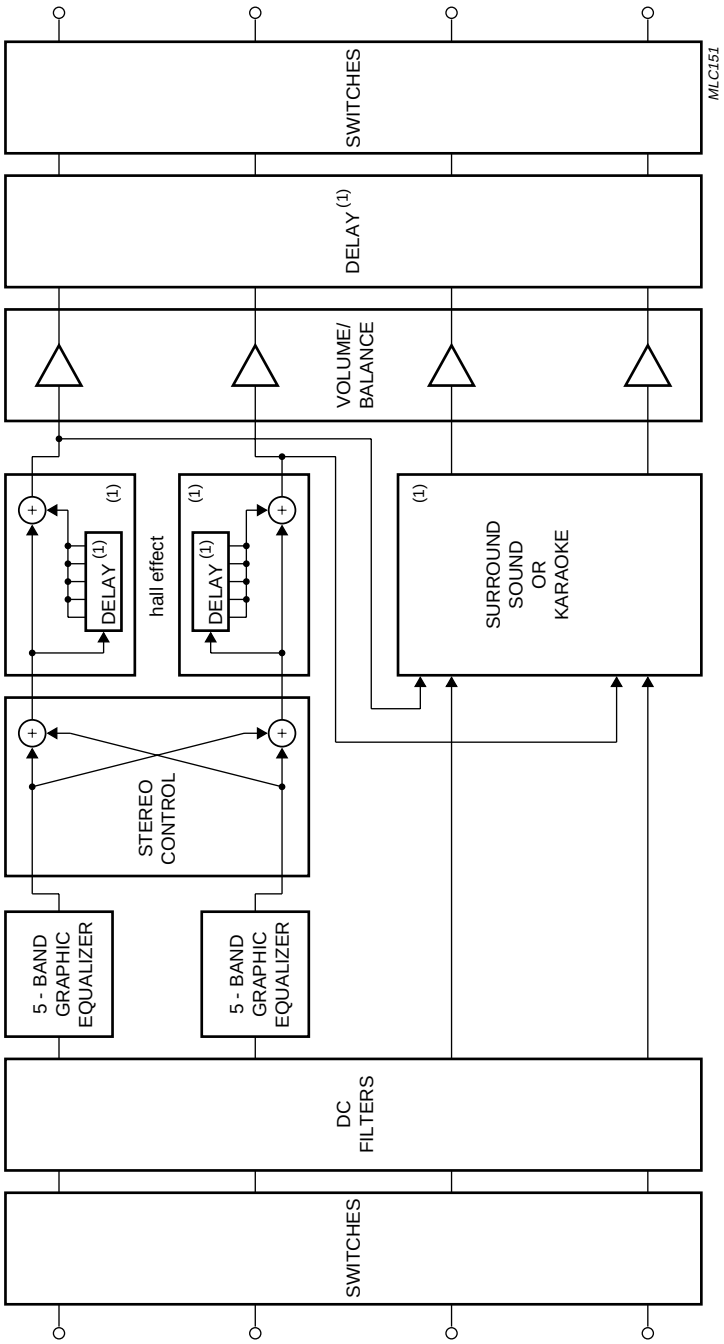


Fig.3 General DAPIC mode with hall-effect.

(1) External DRAM.

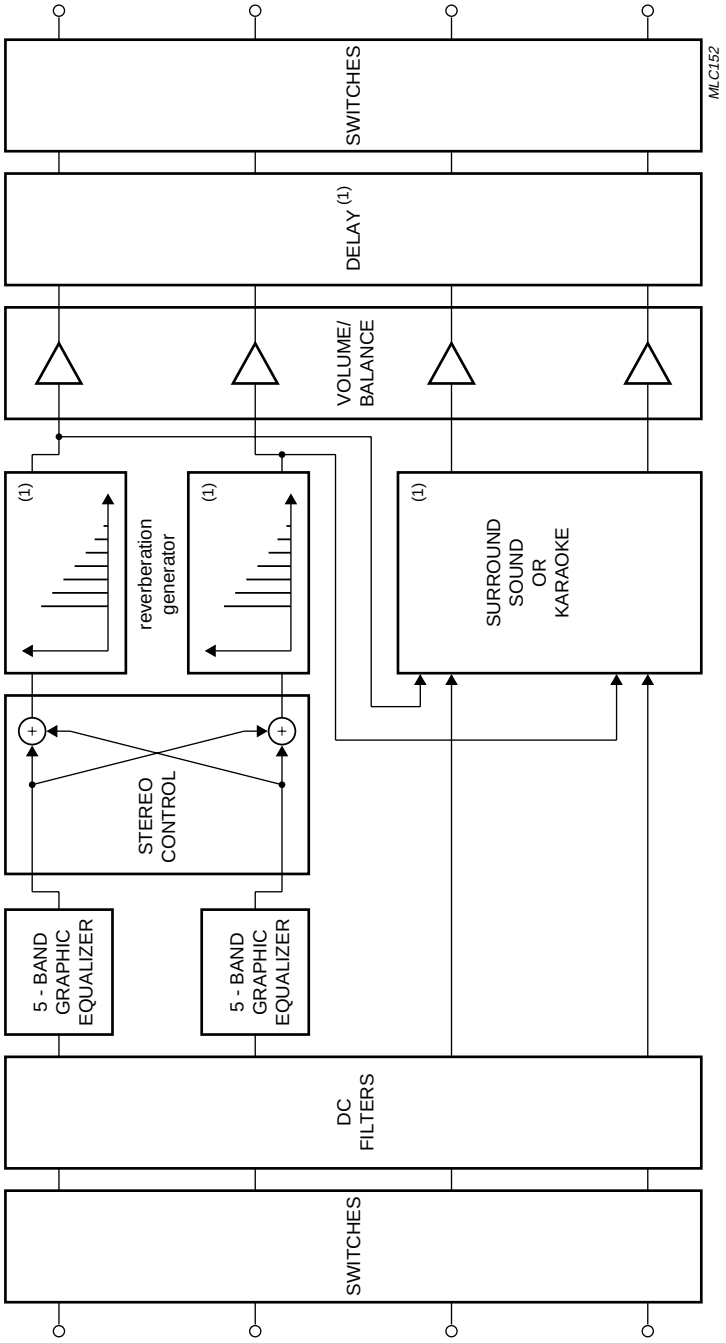


Fig.4 General DAPIC mode with reverberation.

(1) External DRAM.

DUAL-FILTER MODE

In the dual-filter mode one mono signal is accepted (see Fig.5) The input can be selected from either one of the 2 stereo inputs (from the left or right input channel). DC filtering is performed at the input before further processing. Two separate corrections, in parallel, can be performed by means of an 8-band graphic equalizer. 16 poles and 16 zeros can be selected arbitrarily from the Z-domain. At the output, one of the channels can be delayed internally by the DAPIC. The two corrected outputs can be added to either one of the two stereo outputs.

The application for this mode is in loudspeaker correction.

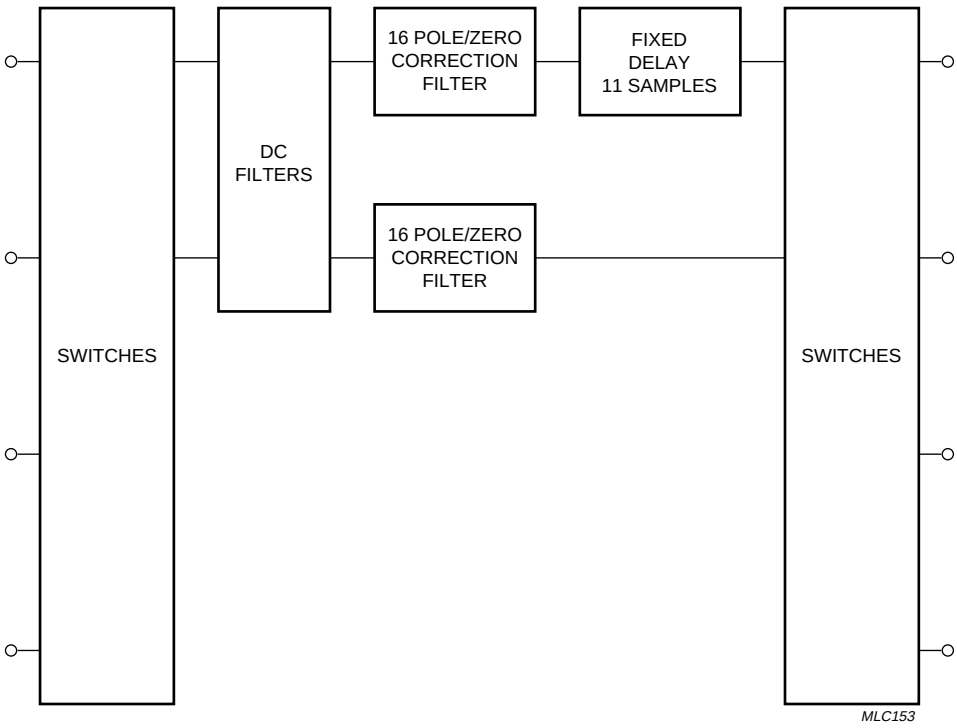


Fig.5 Dual filter mode.

QUAD-FILTER MODE

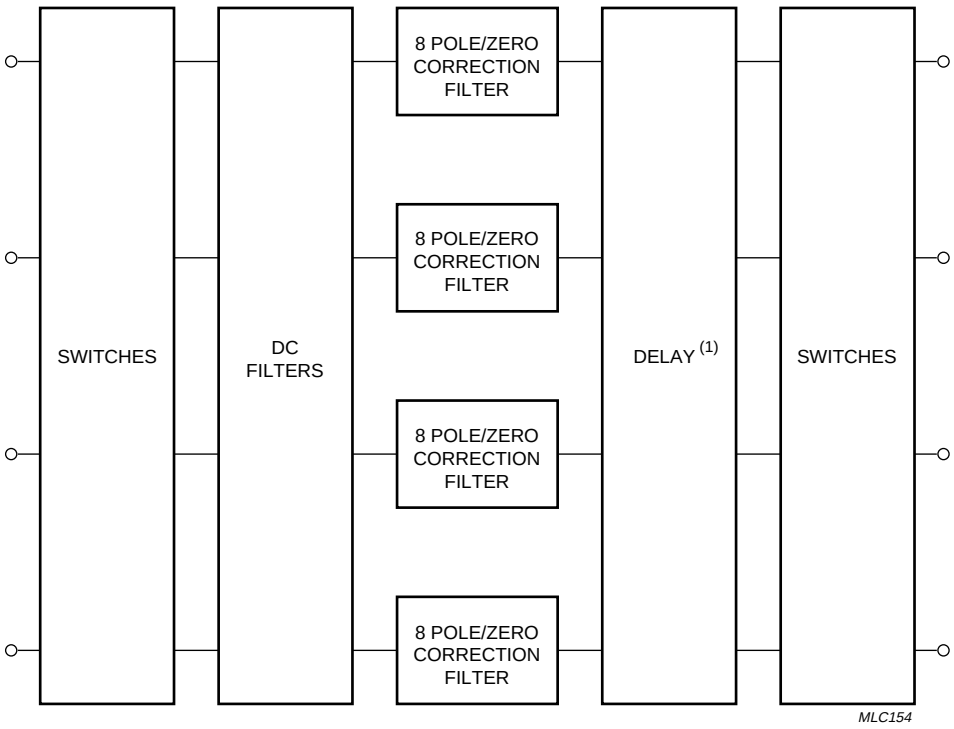
In the quad-filter mode two stereo signals are accepted (see Fig.6). DC filtering is performed at the inputs before further processing. A correction can be performed on the input signals using a 4-band graphic equalizer, i.e. 8 poles and 8 zeros can be placed arbitrarily in the Z-domain. At the output, different delays can be applied to the 4 channels via the external DRAM. The interfacing and addressing of the DRAM is performed by the DAPIC.

The application for this mode is in 4-channel correction applications such as car and home audio systems.

STEREO EXPANSION MODE

In the stereo expansion mode one stereo signal is accepted (see Fig.7). DC filtering is performed at the inputs before further processing. A 4-band graphic equalization is first performed after which a complex stereo expansion is applied. A room effect can be added by the addition of early reflections.

The applications for this mode are in the headphone out-of-head and incredible stereo applications.



(1) External DRAM.

Fig.6 Quad filter mode.

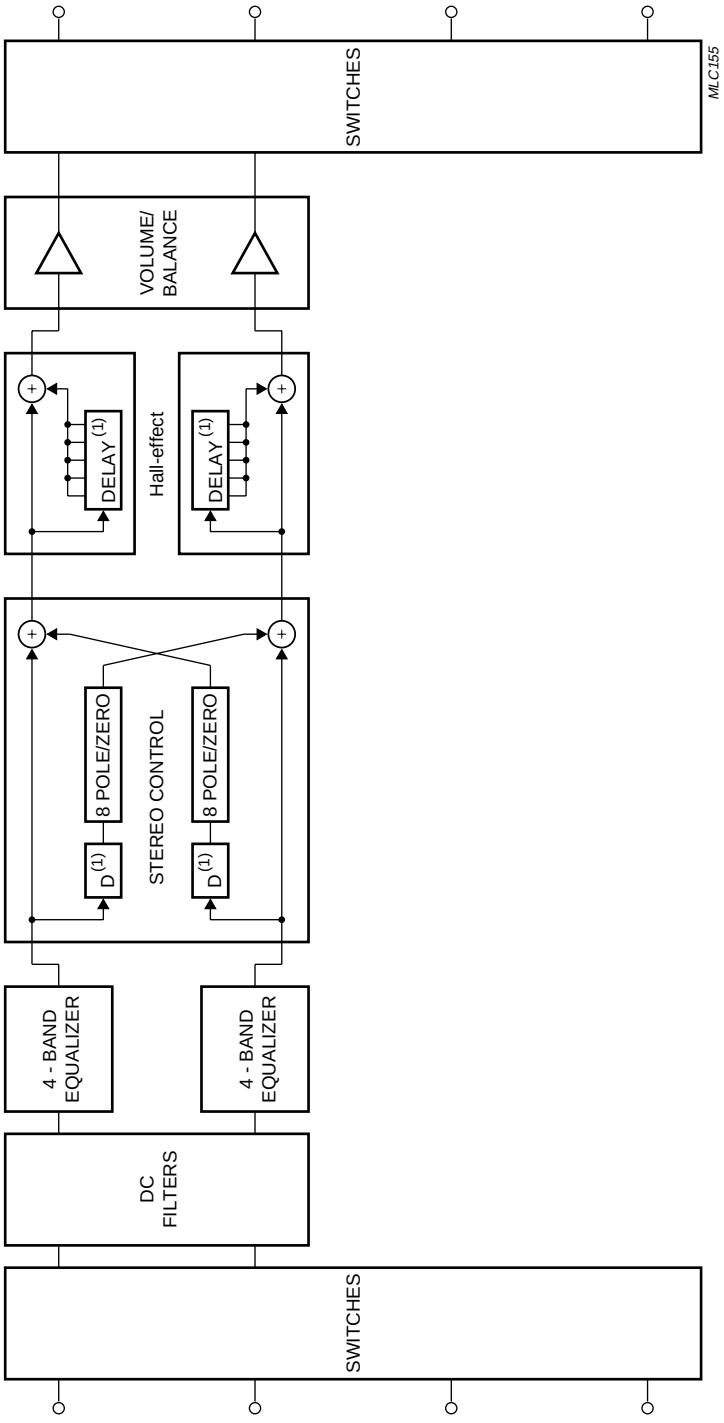


Fig.7 Stereo expansion mode.

(1) External DRAM.

FUNCTIONAL DESCRIPTION

The SAA7740H is used as a slave device. The internal operation is automatically synchronized with the word select clock of the incoming data (I^2S-bus format). Within an input frame of data, at f_{as}, 384 clock cycles are needed to compute a stereo output sample. The external clock therefore, should be minimum $384f_{as}$. External clocks which generate more than 384 clocks cycles will cause the processor to return to a wait state.

The external clock can be either a crystal connected directly to the DAPIC, or any clock generated in the system which contains DAPIC.

The I^2S-bus

Two I^2S-bus inputs and outputs are available on the DAPIC. The serial clock (DIBCK and DOBCK) and the word select (DIWS and DOWS) are applied from an external source. The two inputs and outputs are fully synchronized. However, the inputs do not have to be synchronized with the outputs. The clock and word select signals can be separated at the input and output.

The input and output buses support word lengths in accordance with the I^2S-bus standard. Up to 20 significant bits can be read by the DAPIC. Zeros will be added at the LSB position should less than 20 bits be applied. If more than 20 bits are applied the extra LSBs will be ignored. The stereo word rate (f_{as}) can be either 32, 44.1 or 48 kHz.

Because the DAPIC is a slave device it can only be connected to a master I^2S-bus transmitter or receiver (see Chapter “Timing characteristics” and Fig.9).

I^2C-bus control (SCL and SDA)

The I^2C-bus interface is used to control the operation of the DAPIC for the audio signal processing and write the coefficients and the external delay line addresses of the different signal processing algorithms. New coefficients are updated in real time to the internal RAM.

The transfer byte organization is as follows:

START condition

First byte (8 bits)

Acknowledge (1-bit)

Second byte (8 bits)

Acknowledge (1-bit)

Third to tenth byte (8 bits)

Acknowledge (1-bit)

STOP condition.

The first byte is the address of the I^2C-bus device being addressed. If the device detects its address it answers with an acknowledge by pulling down the data line (SDA) for one clock period (SCL line). The second byte contains the address of the internal RAM to which the first new coefficient should have written. The data will then be transmitted. Each new word (coefficient) is 2 bytes wide. Up to four words of data can be written within one transfer. Should the mode of the feature register be addressed then only one data word will be transferred.

Because the I^2C-bus (on the DAPIC) is a slave receiver bus, the clock has to be generated by the host microcontroller.

The minimum time interval between two I^2C-bus transfers (bus free between a STOP and START condition) should be: $t_{inv} > \left(\frac{coeff + 1}{f_{as}}\right) ms$

Where:

Number of coefficients = coeff

Frequency f_{as} should be in kHz.

Table 1 I^2C-bus slave address.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	1	1	0	AS2(1)	AS1(1)	0

Note

1. AS1 and AS2 are the hardware (pin) programmable address bits. When the device detects this address it will respond with an acknowledge pulse on the SDA line.

Improper acknowledge generated by the DAPIC

If an I²C-bus device, other than DAPIC, is addressed by the master then the DAPIC will generate a short acknowledge pulse. The DAPIC starts pulling down the SDA line at the trailing edge of the SCL clock pulse. and releases the SDA line approximately 390 ns after the leading edge of the following SCL LOW-to-HIGH transition (see Fig.8).

This improper acknowledge pulse can cause the I²C-bus master to detect an incorrect acknowledgement, depending on the capturing moment of the SDA line by the I²C-bus master. Any possible non-acknowledgements of involved I²C-bus devices, including the SAA7740H, will be masked thus making the system unreliable.

To avoid these problems the I²C-bus master should only capture the SDA line at such a moment that the improper acknowledge pulse will not be detected.

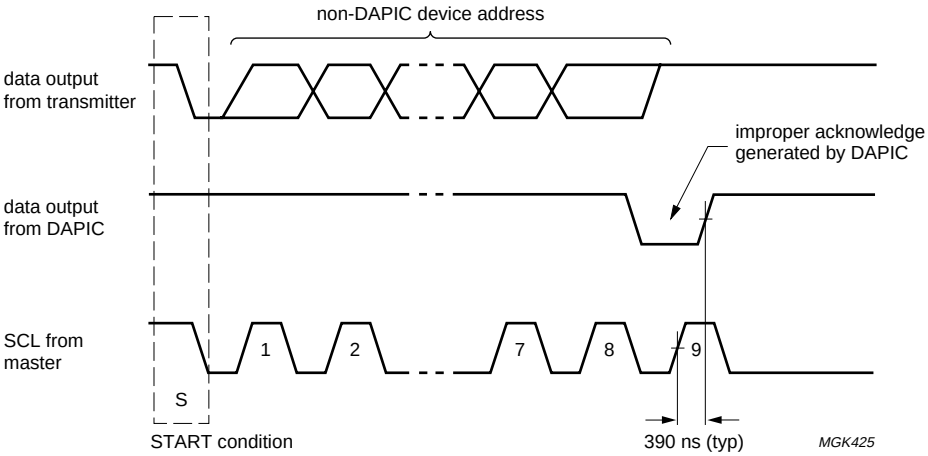


Fig.8 Improper acknowledge generated by the DAPIC.

DRAM interface

The DRAM interface contains a nibble wide data bus, a 9-bit wide address bus and all necessary control signals to enable the different DRAM configurations.

Timing of the control signals $\overline{RAS}$, $\overline{CAS}$, $\overline{CAS2}$, A8B, $\overline{OE}$ and $\overline{WE}$ is related to the applied clock frequency of the DAPIC. The important timing parameters are the page mode cycle time ($t_{cy;CAS}$), the access time ($t_{acc;RAS}$), the refreshing rate and the maximum value for $\overline{RAS}$ to $\overline{CAS}$ delay time ($t_{dRAS;CAS}$) (see Chapter “Timing characteristics” and Fig.10). A read/write operation will always be executed in the page mode (one row address and four column addresses) because every data transfer consists of 4 nibbles.

The refresh time of the DRAM (t_{rfsh}) must be greater than;

$$t_{rfsh} > \left(\frac{2^{addr}}{3f_{as}}\right) ms$$

where ‘addr’ is the number of physical address lines and f_{as} is measured in kHz.

For fast DRAMs, the maximum value for $\overline{RAS}$ to $\overline{CAS}$ delay time ($t_{dRAS;CAS}$) is important.

Different DRAM combinations can be connected to the DAPIC. The smallest DRAM is a 64×4-bit (256 kbits) RAM. For this configuration, 16K data words can be stored. When this RAM is connected to the DAPIC, the MSB address signal (A8) can be felt floating.

The DAPIC can address up to 1 Mbit DRAMs. However, RAMs greater than 1 Mbit can also be connected. This, therefore, implies that the redundant address lines of the RAM must be fixed to V_{DD} or V_{SS} or must be joined with one of the other address pins.

The choice of a 256 kbit or a 1 Mbit DRAM device must be indicated by a flag bit residing in the start address control word of the different delay lines.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	DC supply voltage (each supply pin)		–0.5	+6.5	V
ΔV_{DD}	voltage difference between V_{DD} and V_{DDX}		–	550	mV
I_{IK}	DC input clamp diode current	$V_I < –0.5$ V or $V_I > V_{DD} + 0.5$ V	–	±10	mA
I_{OK}	DC output clamp diode current (output type 4 mA)	$V_O < –0.5$ V or $V_O > V_{DD} + 0.5$ V	–	±20	mA
I_O	DC output sink or source current (output type 4 mA)	$–0.5 < V_O < V_{DD} + 0.5$ V	–	±20	mA
I_{DD}	DC supply current per pin		–	50	mA
I_{SS}	DC supply current per pin		–	50	mA
LTCH	latch-up protection	CIC specification/test method	100	–	mA
P_O	power dissipation per output		–	100	mW
P_{tot}	total power dissipation		–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es}	electrostatic discharge	note 1	–3000	+3000	V
		note 2	–300	+300	V

Notes

1. Human body model: C = 100 pF; R = 1.5 kΩ.
2. Machine model: C = 200 pF; L = 2.5 μH; R = 0 Ω.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	47	K/W

DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDn}	DC supply voltage (pins 7, 8, 26, 32, 38, 53, 54 and 60)		4.5	5.0	5.5	V
$I_{DD(tot)}$	total of all DC supply current pins	f_{xtal} = 16.9344 MHz	–	60	–	mA
P_{tot}	total power dissipation	f_{xtal} = 16.9344 MHz	–	300	–	mW
V_{IH}	HIGH level input voltage (pins 1, 3, 4, 11, 12, 15, 16, 36, 37, 41 to 45, 47 to 49, 51, 52, 62 and 64)		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage (pins 1, 3, 4, 11, 12, 15, 16, 36, 37, 41 to 45, 47 to 49, 51, 52, 62 and 64)		–	–	$0.3V_{DD}$	V
$V_{th(pos)}$	Schmitt trigger positive-going threshold (pin 2)		–	–	$0.8V_{DD}$	V
$V_{th(neg)}$	Schmitt trigger negative-going threshold (pin 2)		$0.2V_{DD}$	–	–	V
V_{hys}	hysteresis voltage (pin 2)		–	$0.33V_{DD}$	–	V
V_{OH}	HIGH level output voltage (pins 10 to 12, 14 to 24, 27 to 31, 33 to 35 and 63)	V_{DD} = 4.5 V; I_O = 4 mA	4.0	–	–	V
V_{OL}	LOW level output voltage (pins 3, 10 to 12, 14 to 24, 27 to 31, 33 to 35 and 63)	V_{DD} = 4.5 V; I_O = 4 mA	–	–	0.5	V
I_{LI}	input leakage current (pins 1, 2, 4, 36, 37, 41 to 45, 47 to 49, 51, 52 and 62)	V_{DD} = 0 or 5.5 V	–	–	±1	µA
I_{ZO}	output leakage current; 3-state (pins 3, 11, 12, 15 and 16)	V_{DD} = 0 or 5.5 V	–	–	±5	µA
R_{pd}	internal pull-down resistance to V_{SS} (pin 64)	$V_I = V_{DD}$	17	–	134	kΩ
$t_{r(i)}$	input rise time	V_{DD} = 5.5 V	–	6	200	ns
$t_{f(i)}$	input fall time	V_{DD} = 5.5 V	–	6	200	ns
$t_{r(o)}$	output rise time for LOW-to-HIGH transition	V_{DD} = 4.5 V; T_{amb} = 85 °C; C_L = pF; pins 11, 12, 15 and 16	–	–	$9.5 + 0.4C_L$	ns
		V_{DD} = 4.5 V; T_{amb} = 85 °C; C_L = pF; pins 10, 14, 17 to 24, 27 to 31, 33 to 35 and 63	–	–	$8.5 + 0.4C_L$	ns
$t_{f(o)}$	output fall time for HIGH-to-LOW transition	V_{DD} = 4.5 V; T_{amb} = 85 °C; C_L = pF; pins 11, 12, 15 and 16	–	–	$11 + 0.5C_L$	ns
		V_{DD} = 4.5 V; T_{amb} = 85 °C; C_L = pF; pins 10, 14, 17 to 24, 27 to 31, 33 to 35 and 63	–	–	$9.0 + 0.5C_L$	ns

AC CHARACTERISTICS

V_{DDX} = 5 V; T_{amb} = +25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{xtal}	crystal input frequency	$\geq 384 f_{as}$	12.288	16.9344	23.0	MHz
α_f	spurious frequency attenuation		20	–	–	dB
I_{59}	crystal current output (pin 59)	slave mode only	–	–	1	mA
g	transconductance at maximum current		–	0.4	–	mS
V_{xtal}	voltage across crystal		–	500	–	mV
C_L	load capacitance		–	–	15	pF
$\frac{1}{2}T_{clk}$	half clock period of external clock		21	–	–	ns

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{HC}	pulse width HIGH, DIBCK and DOBCK	110	–	ns
t_{LC}	pulse width LOW, DIBCK and DOBCK	110	–	ns
t_r	DIBCK and DOBCK rise time	–	20	ns
t_f	DIBCK and DOBCK fall time	–	20	ns
t_{h1}	DIWS and DOWS hold time	10	–	ns
t_{su1}	DIWS and DOWS set-up time	20	–	ns
t_{h2}	DI1D and DI2D hold time	10	–	ns
t_{su2}	DI1D and DI2D set-up time	20	–	ns
t_{acc}	DO1D and DO2D access time	–	$25 + 0.5C_L$ (C_L in pF)	ns
DRAM timing				
$\frac{1}{2}T_{clk}$	half clock period	21	–	ns
$t_{p;\overline{RAS}}$	$\overline{RAS}$ precharge time	$4 \times \frac{1}{2}T_{clk} - 12$	–	ns
$t_{W;\overline{RAS}}$	$\overline{RAS}$ pulse width	$16 \times \frac{1}{2}T_{clk} - 12$	–	ns
$t_{su;RA}$	row address set-up time	$\frac{1}{2}T_{clk} - 8$	–	ns
$t_{h;RA}$	row address hold time	$\frac{1}{2}T_{clk} - 12$	–	ns
$t_{d\overline{RAS};\overline{CAS}}$	$\overline{RAS}$ to $\overline{CAS}$ delay time	$2 \times \frac{1}{2}T_{clk} - 11$	$2 \times \frac{1}{2}T_{clk} + 14$	ns
$t_{h;\overline{CAS}}$	$\overline{CAS}$ hold time	$4 \times \frac{1}{2}T_{clk} - 12$	–	ns
$t_{h;RAS}$	$\overline{RAS}$ hold time	$2 \times \frac{1}{2}T_{clk} - 12$	–	ns
$t_{\overline{RAS};CA}$	$\overline{RAS}$ to column address	–	$\frac{1}{2}T_{clk} + 8$	ns
$t_{hCA;\overline{RAS}}$	column address hold time from $\overline{RAS}$	$5 \times \frac{1}{2}T_{clk} - 11$	–	ns
$t_{hCA;\overline{RAS}p}$	column address hold time from $\overline{RAS}$ precharge	$\frac{1}{2}T_{clk} - 12$	–	ns
$t_{lCA;\overline{RAS}}$	column address to $\overline{RAS}$ lead time	$3 \times \frac{1}{2}T_{clk} - 8$	–	ns
$t_{p\overline{CAS};\overline{RAS}}$	$\overline{CAS}$ to $\overline{RAS}$ precharge time	$4 \times \frac{1}{2}T_{clk} - 14$	–	ns
$t_{su;CA}$	column address set-up time	$\frac{1}{2}T_{clk} - 8$	–	ns

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{h1CA;\overline{CAS}}$	column address hold time to $\overline{CAS}$	$3 \times \frac{1}{2}T_{clk} - 14$	–	ns
$t_{h2CA;\overline{CAS}}$	column address hold time to $\overline{CAS}$ precharge	$\frac{1}{2}T_{clk} - 15$	–	ns
$t_{W;\overline{CAS}}$	$\overline{CAS}$ pulse width	$2 \times \frac{1}{2}T_{clk} - 14$	–	ns
$t_{p;\overline{CAS}}$	$\overline{CAS}$ precharge time	$2 \times \frac{1}{2}T_{clk} - 11$	–	ns
$t_{cy;\overline{CAS}}$	$\overline{CAS}$ page mode cycle time	$4 \times \frac{1}{2}T_{clk}$	–	ns
$t_{acc;CA}$	access time from column address	–	$3 \times \frac{1}{2}T_{clk} - 20$	ns
$t_{acc;\overline{CAS}}$	access time from $\overline{CAS}$	–	$2 \times \frac{1}{2}T_{clk} - 24$	ns
$t_{acc;\overline{RAS}}$	access time from $\overline{RAS}$	–	$4 \times \frac{1}{2}T_{clk} - 22$	ns
$t_{hDAT;\overline{CAS}}$	data hold time from $\overline{CAS}$	2	–	ns
$t_{rcy;def}$	read cycle definition time	$4 \times \frac{1}{2}T_{clk} - 10$	–	ns
$t_{su;DAT}$	data input set-up time	$\frac{1}{2}T_{clk} - 8$	–	ns
$t_{h;DAT}$	data input hold time	$3 \times \frac{1}{2}T_{clk} - 16$	–	ns
$t_{hDAT;\overline{RAS}}$	data input hold time from $\overline{RAS}$	$5 \times \frac{1}{2}T_{clk} - 15$	–	ns
$t_{wcy;def}$	write cycle definition time	$2 \times \frac{1}{2}T_{clk} - 12$	–	ns
t_{off}	output data disable time	–	$\frac{1}{2}T_{clk} + 8$	ns

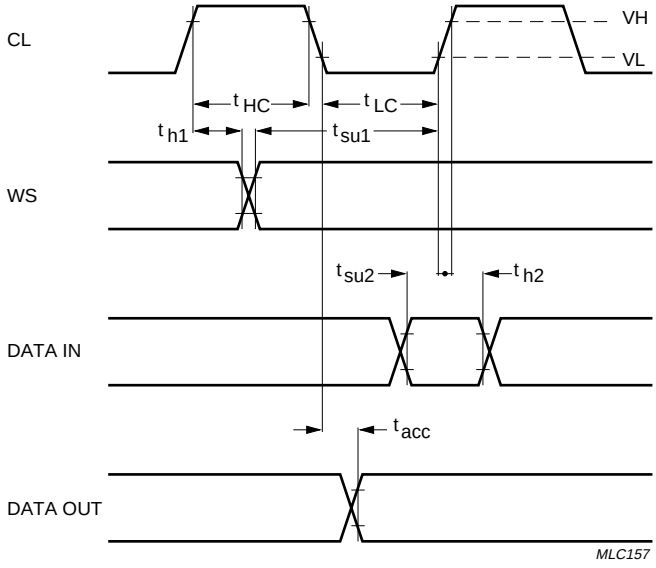


Fig.9 I²S-bus timing diagram.

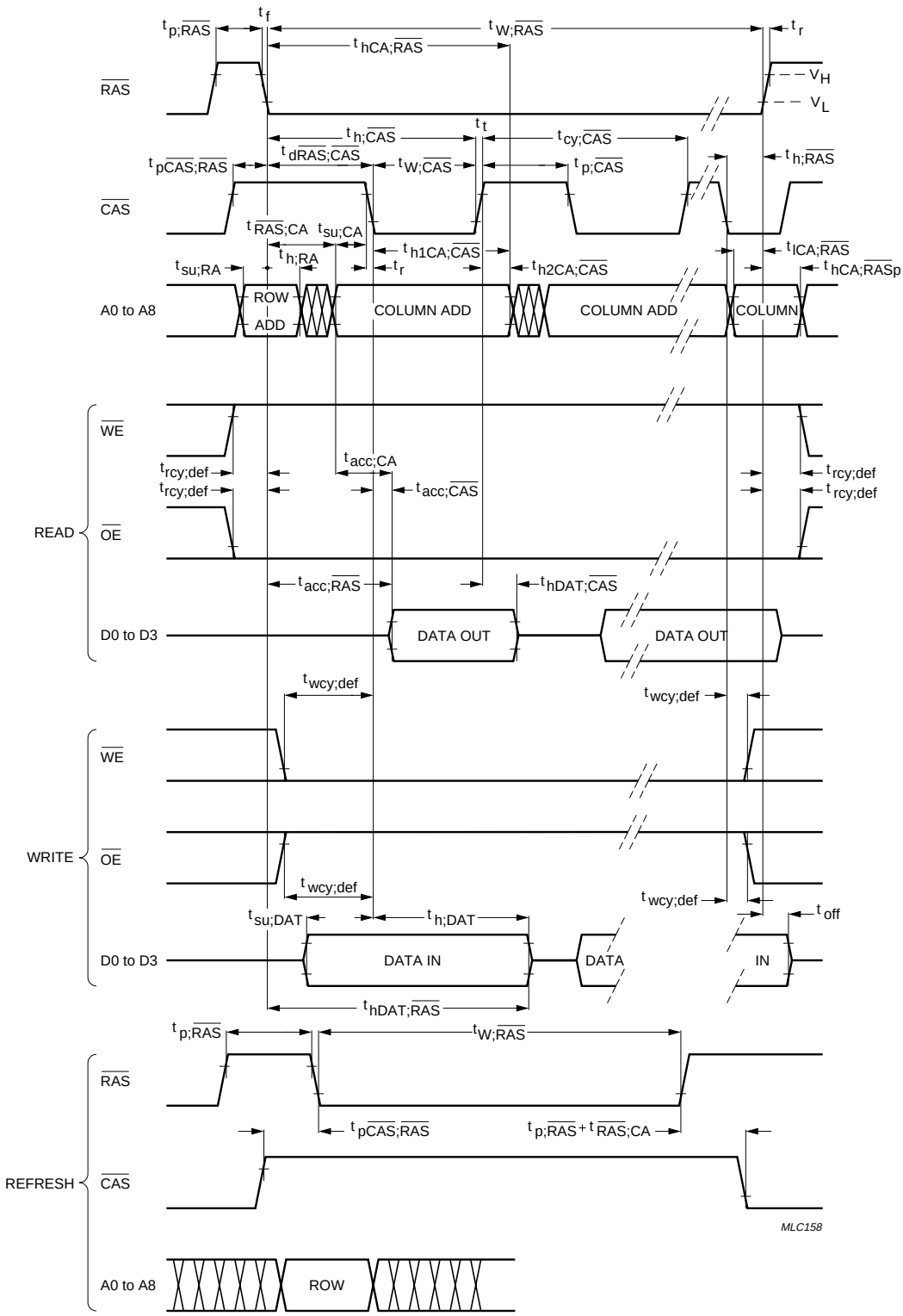


Fig.10 Timing diagram DRAM interface.

I²S-BUS PROTOCOL

The I²S-bus digital interface is used for communication to external digital sources. It is a 3-line serial bus with one line each for data, clock and word select. Figure 11 illustrates an excerpt from the Philips I²S-bus specification interface report with respect to general timing and format of the bus. Word select (WS) at logic 0 signifies the left channel and logic 1 the right channel.

The serial data is transmitted in two's complement with MSB first. One clock period after the negative edge of the WS line, the MSB of the left channel is transmitted. Data is synchronized on the negative edge of the clock and latched on the positive edge.

Two data line have been implemented as input from an external processor for the four audio channels. Because of this configuration the DAPIC operates in the following manner.

The I²S-bus input block reads 4 samples (left and right samples of the front and rear channel) and stores the information into the register file. The operators read from the register file, process the data and store the intermediate results back into the register file. If a delay line is required, the external RAM will need to be accessed. The output samples are read from the register file and are passed via the fade unit to the I²S-bus output block. The same operation is repeated for each incoming audio sample.

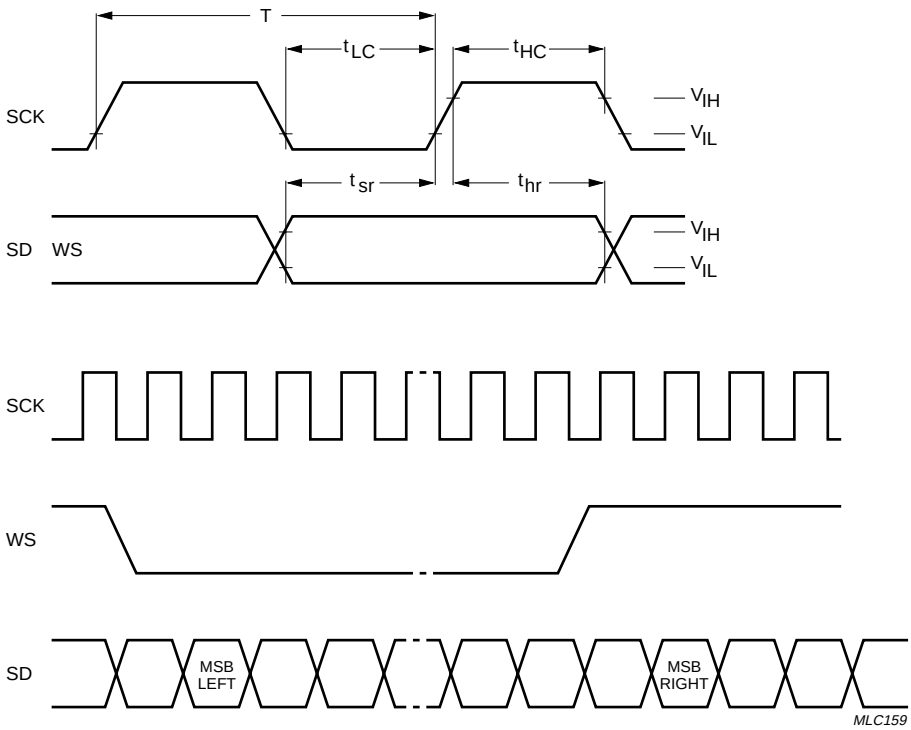


Fig.11 I²S-bus timing format.

I²C-BUS PROTOCOL

The I²C-bus is intended for 2-way, 2-line communication between different ICs or modules. The two lines are the serial data line (SDA) and the serial clock line (SCL). Both lines must be connected to the supply rail via a pull-up resistor when connected to the output stages of a microcontroller. Data transfer can only be initiated when the bus is not busy. Full details of the I²C-bus are given in the document *"The I²C-bus and how to use it"*. This document may be ordered using the code 9398 393 40011.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulses as changes in the data line at this time will be interpreted as control signals. The maximum clock frequency is 100 kHz (see Fig.12).

START and STOP condition

In the START and STOP condition the data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the STOP condition (P); (see Fig.13).

Data transfer

A device generating a message is a 'transmitter', a device receiving a message is a 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the device are the 'slaves' (see Fig.14).

Acknowledge

The number of data bytes that are transferred between the START and STOP conditions, from transmitter to receiver, is unlimited. Each byte is followed by an acknowledge bit. The acknowledge bit is a HIGH level bit placed on the bus by the transmitter, whereas the master generates an extra acknowledge bit which is related to the clock pulse. A slave receiver which is addressed must generate an acknowledge bit after the reception of each byte. The master must also generate an acknowledge bit after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Set-up and hold times must also be taken into account. A master receiver must signal an end-of-data to the transmitter. This is achieved by not generating an acknowledge on the last byte that has been clocked out of the slave. In this condition the transmitter must leave the data line HIGH to enable the master to generate a STOP condition (see Fig.15).

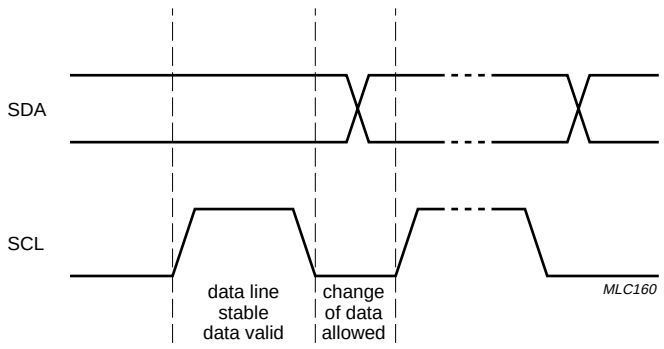


Fig.12 Bit transfer on the I²C bus.

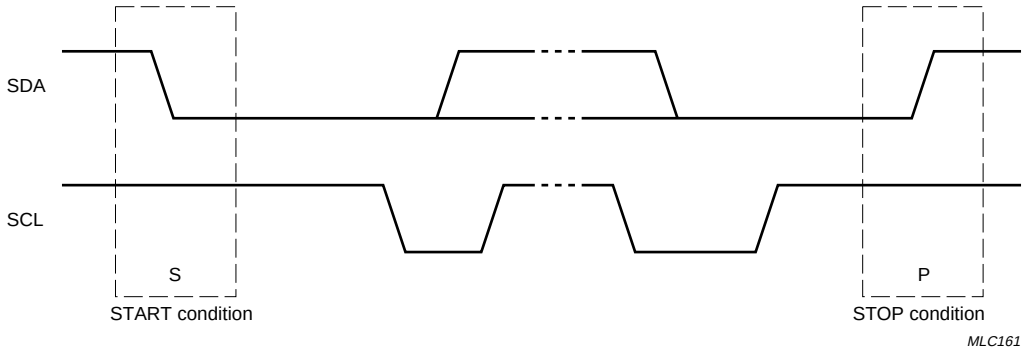


Fig.13 START and STOP conditions.

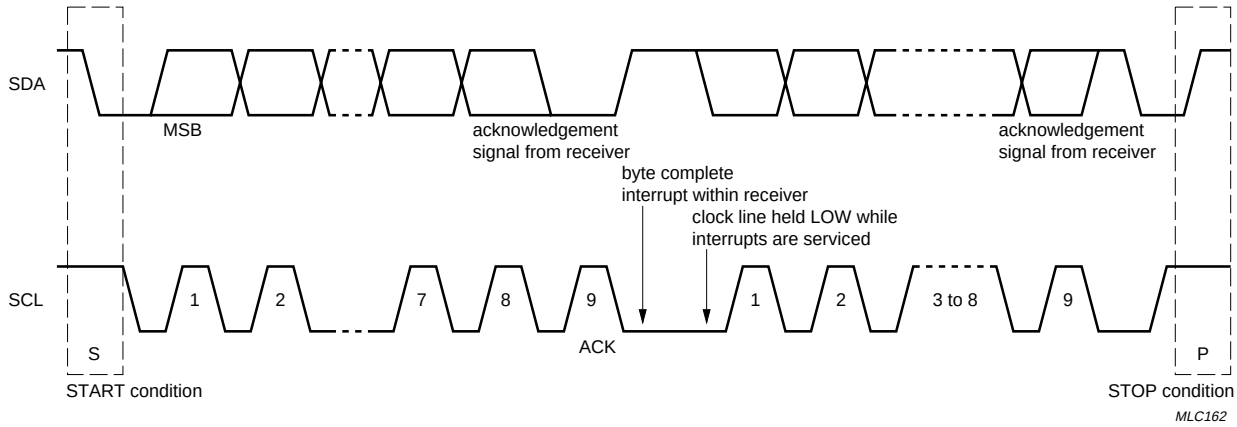


Fig.14 Data transfer on the I^2C-bus.

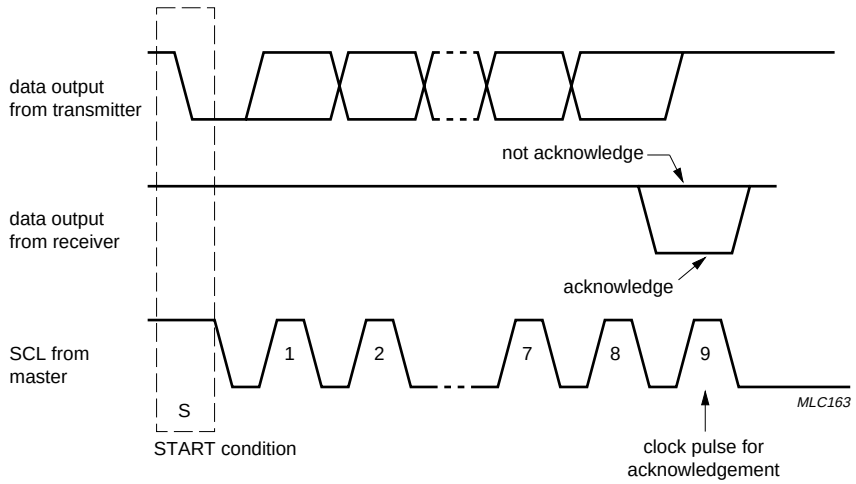


Fig.15 Acknowledge on the I^2C-bus.

APPLICATION INFORMATION

Clock circuit and oscillator

The clock generation of the SAA7740H is designed to accommodate two main modes, the master and the slave.

In the master mode, the DAPIC is the master in the system. The clock is generated by connecting a crystal to the oscillator pins CLK1/XTAL1 and XTAL2 (see Fig.16).

In the slave mode, the DAPIC is supplied as a slave. The external clock should be connected to the oscillator at pin CLK1/XTAL1 (see Fig.17).

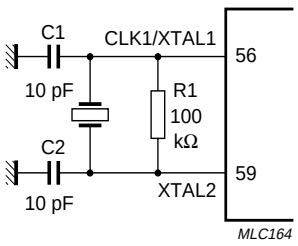


Fig.16 Master mode.

Crystal oscillator supply

The power supply for the oscillator is separate from the other supply line. This is to minimize feedback from the ground bounce of the IC to the oscillator. Pin V_{SSX} is the ground supply and V_{DDX} is the positive supply.

Power supply connection and EMC

The SAA7740H has in total 8 positive supply lines (V_{DD}) including V_{DDX}, and 8 ground supply lines (V_{SS}) including V_{SSX}. For correct current distribution all positive supply lines should be connected together on the printed circuit-board. The ground supply lines should also be connected together on the printed circuit-board.

To minimize radiation the IC should be placed on a double-layer printed circuit-board with a large ground plane on one side. The ground supply lines should have a short connection to the ground plane. An LC network in the positive supply lines can be used as a high frequency filter.

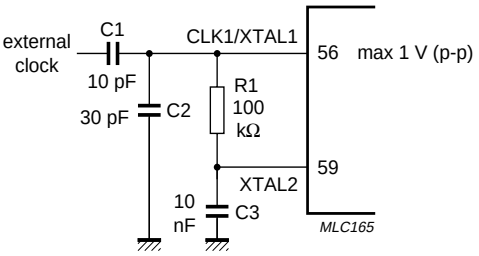


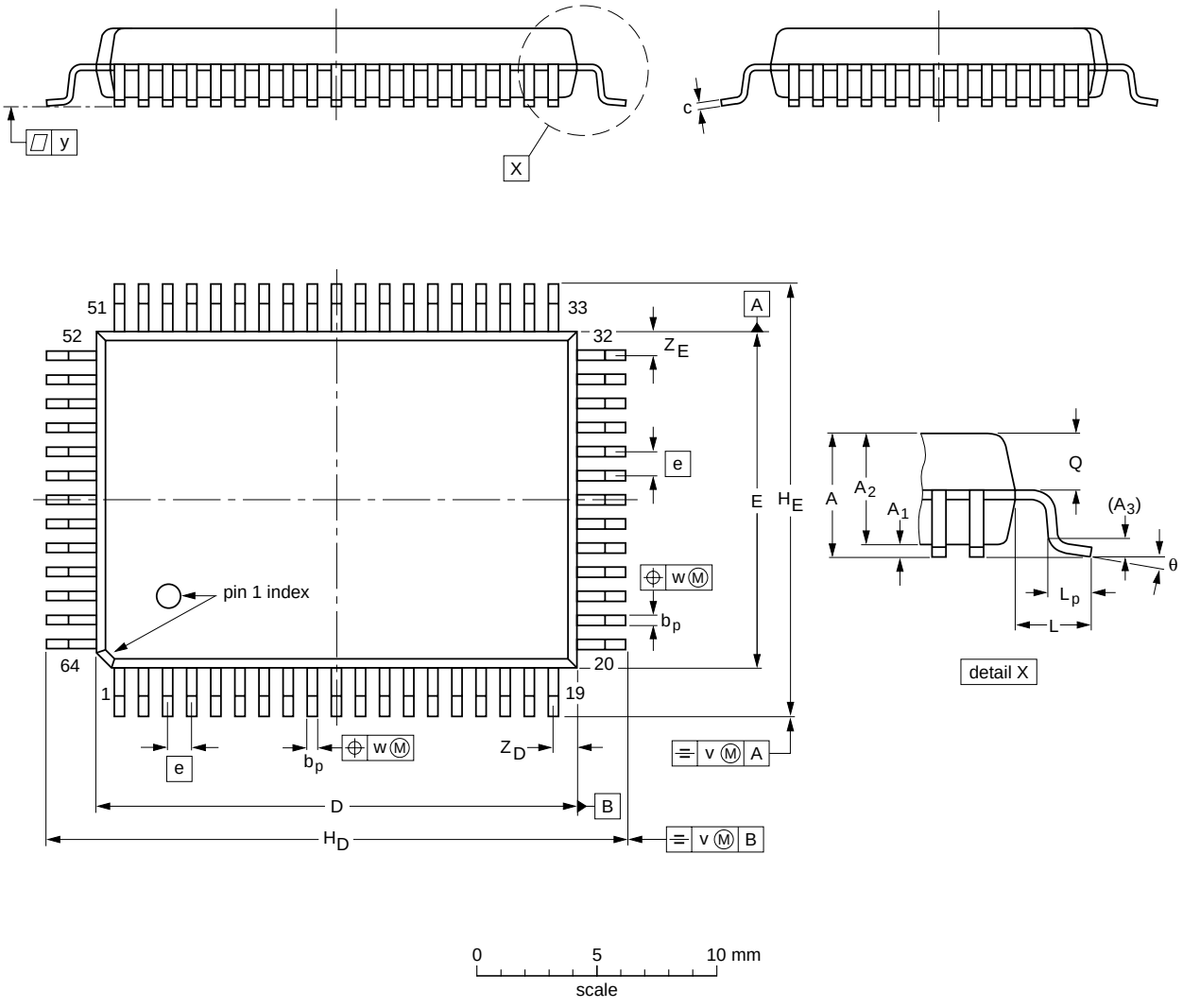
Fig.17 Slave mode.

Test mode connections

Pins SCCLK, TSTCLK, TST1, TST2 and TST3 are used to put the IC in the test mode and to test the internal connections. In the application these pins must be connected to ground.

PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT319-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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